CLAIMS

1. A method for operating a driver circuit, comprising:
operating the driver circuit at full power in a dynamic mode; and
operating the driver circuit at reduced power in a termination mode.

2. A method as defined in claim 1, wherein operating the driver circuit at reduced power comprises reducing or turning off at least one current in the driver circuit in the termination mode.

3. A method as defined in claim 1, wherein operating the driver circuit at reduced power comprises reducing a slew current for an output stage of the driver circuit.

4. A method as defined in claim 1, wherein operating the driver circuit at reduced power comprises reducing an idle current for an output stage of the driver circuit.

5. A method as defined in claim 1, wherein operating the driver circuit at reduced power comprises reducing a slew current for an output stage of the driver circuit, further comprising maintaining an idle current for the output stage at a constant level in the dynamic mode and in the termination mode.

6. A method as defined in claim 1, wherein operating the driver circuit at reduced power comprises reducing bias current to a reverse buffer of the driver circuit.

7. A method as defined in claim 1, wherein operating the driver circuit at reduced power comprises reducing bias current to a digital input circuit of the driver circuit.

8. A method as defined in claim 1, wherein operating the driver circuit at reduced power comprises reducing bias current to input buffers that supply programmable levels to an output stage of the driver circuit.

9. A method as defined in claim 1, wherein operating the driver circuit at reduced power comprises reducing bias current to a cable loss compensation circuit of the driver circuit.

10. A method as defined in claim 1, wherein operating the driver circuit at reduced power comprises reducing at least one bias current to the driver circuit using a current multiplier.

11. A method as defined in claim 1, wherein operating the driver circuit at full power comprises selectably operating in a high state, a low state or an inhibit state in the dynamic mode.

12. A method as defined in claim 1, wherein operating the driver circuit at reduced power comprises selectably operating in a high state, a low state or an inhibit state in the termination mode.

13. A driver circuit including mode control circuitry for selectably operating at full power in a dynamic mode and for operating at reduced power in a termination mode.

14. A driver circuit as defined in claim 13, wherein the mode control circuit comprises a current multiplier and a switching circuit for switching a control current supplied to the current multiplier based on the dynamic mode or the termination mode.

15. A driver circuit as defined in claim 13, wherein the mode control circuit is configured to reduce at least one current in the driver circuit in the termination mode.

16. A driver circuit for use in automatic test equipment, comprising:

an output circuit operable in a dynamic mode and in a termination mode; and

a mode control circuit for supplying a first current to the output circuit in the dynamic mode and for supplying a second current to the output circuit in the termination mode in response to a mode select signal.

17. A driver circuit as defined in claim 16, wherein the mode control circuit comprises a current multiplier and a switching circuit for switching a control current supplied to the current multiplier in response to the mode select signal.

18. A driver circuit as defined in claim 17, wherein the first current includes a dynamic mode current plus a standby current and wherein the second current includes the standby current.

19. A driver circuit as defined in claim 17, wherein an output current of the current multiplier is about 2 to 30 times the control current.

20. A driver circuit as defined in claim 16, wherein the output circuit comprises a class AB output circuit.

21. A driver circuit as defined in claim 16, wherein the mode control circuit is configured to control a slew current supplied to the output circuit in response to the mode select signal.

22. A driver circuit as defined in claim 16, wherein the mode control circuit is configured to control an idle current supplied to the output circuit in response to the mode select signal.

23. A driver circuit as defined in claim 16, wherein the mode control circuit is configured to reduce a slew current for the output circuit in the termination mode and to maintain an idle current for the output circuit at a constant level in the dynamic mode and in the termination mode.

24. A driver circuit as defined in claim 16, further comprising a reverse buffer coupled to the output circuit, wherein the mode control circuit is configured to control a bias current supplied to the reverse buffer in response to the mode select signal.

25. A driver circuit as defined in claim 16, further comprising a digital input circuit coupled to the output circuit, wherein the mode control circuit is configured to control a bias current supplied to the digital input circuit in response to the mode select signal.

26. A driver circuit as defined in claim 16, further comprising one or more input buffers coupled to the output circuit, wherein the mode control circuit is

configured to control a bias current supplied to the one or more input buffers in response to the mode select signal.

27. A driver circuit as defined in claim 16, further comprising a cable loss compensation circuit coupled to the output circuit, wherein the mode control circuit is configured to control the bias current supplied to the cable loss compensation circuit in response to the mode select signal.

28. A method for operating a driver circuit in automatic test equipment, comprising:

operating an output circuit of the driver circuit in a dynamic mode and in a termination mode in response to a mode select signal;

supplying a first current to the output circuit in the dynamic mode; and

supplying a second current to the output circuit in the termination mode, wherein the first current is larger than the second current.